IN THE SPECIFICATION

Please amend paragraph [0058] as follows:

[0058] Figure 4, details a simplified diagram of a split data move control circuit 400 of a memory system or memory controller embodiment of the present invention. The split data move control circuit 400 operates with the data splitting hardware (such as is disclosed in U.S. Patent Application No. 10/602,991 ~~(Attorney Docket No. 400.197US01)~~, titled "Erase Block Data Splitting", filed June 24, 2003, and which issued on June 14, 2005 as U.S. Patent No. 6,906,961) and allows for automating of a split data move operation with automatic generation of sequential target addresses and masking of data given a starting address loaded into it by a processor or a memory controller. This simplifies the memory system address control in a move operation in a data splitting memory or memory system. It is noted that a non-split data move control circuit based off the split data move control circuit 400 of Figure 4 for embodiments of the present invention is possible and should be apparent to those skilled in the art with the benefit of the present disclosure.